REMARKS

The claims have been amended substantially as suggested by the Examiner to overcome the minor points of consistency and proper punctuation.

Claim 1 has been amended to address the examiner's rejection under 35 U.S.C 112 that Claims 1 to 3 are rejected as indefinite due to not clarifying when or how multiple input signals are simultaneously synchronized.

The Examiner will appreciate that, as explained at page 8, line 20 et seq. of the specification, the multiple input signals are simultaneously synchronized by clocking the calculations of a single time-sliced discrete time PLL at a high enough rate such that every input signal sample can be serviced and the DPLL can accommodate all calculation requests from the input signals. Such a method requires that any registered delay elements within the DPLL architecture have their values stored within the context memory for each and every signal pair.

Claim 1 has been amended to make this clear.

The Examiner has rejected Claim 1 under 35 U.S.C.103 based on a combination of Pinto and Yamashita.

Claim 1 has been amended to make clear that the "PLL is arranged to carry out a calculation for each of the signal pairs."

Pinto et al presents a PLL that can be tuned and thus optimized to a variety of input signal types. However, a separate and distinct PLL, in hardware, must be used for each and every input signal.

Pinto seeks to optimize each PLL for the particular input signal that

the PLL concerned sees while in operation such that the PLL operates in a linear region with wide dynamic range. Nevertheless, that PLL can only be used for one such input signal at a time while in operation.

The present invention, as now clearly defined in claim 1, provides a single PLL that can be used to synchronize to multiple input clock signals while this single PLL is in operation. This is accomplished by applying a context memory to store a complete history data for each input signal and clocking the control logic at a higher rate than the incoming input signal samples such that the single PLL hardware is available to calculate upon and synchronize each and every input signal simultaneously. Hence, the PLL hardware is time-sliced.

Pinto can optimize a PLL to a multitude of input signal types, but only one input signal per PLL while in operation. The present invention shares a single PLL to synchronize to a multitude of input signals while in operation.

Thus, Pinto does not disclose a method of simultaneously synchronizing multiple extracted input clock signals to multiple output clock signals. Instead Pinto provides a method by which the PLL can be tuned to the characteristics of multiple input signal types to operate the VCO in an ideal range. This cannot however be applied to multiple input signals simultaneously.

This is clear from the three objects set out in column 1, lines 50 to 63 of Pinto.

The Examiner has combined in respect of original Claim 1, Pinto with the Japanese reference of Yamashita.

Yamashita discloses a PLL containing a history function used to

store previous VCO control variables as hysteric information and thereby improve the efficiency of the PLL. This is accomplished by subsequently routing the phase contrast output by the phase comparator to the controller. The controller then reads the hysteric control variable information relating to that phase contrast output from memory and applies this to the VCO. (see sections 008 to 0011). Presumably a lower cost and lower power PLL is derived by using this memory lookup method between phase contrast and VCO control voltage history rather than persistently calculating a new phase detector output, loop filter output, and VCO input as in a prior art PLL.

However Yamashita does not disclose nor suggest the concept of the present invention of using a single PLL to synchronize multiple input signals simultaneously through the use of high speed control logic and context memory.

Both Pinto and Yamashita thus disclose improvements in a PLL by which it can operate more effectively with a single input signal. Thus combining Pinto and Yamashita would also merely provide some combination of arrangements which allow the PLL to operate more effectively with a single input signal. Nothing in this combination would n any way suggest the concept of using this single PLL to synchronize multiple input signals simultaneously through the use of high speed control logic and context memory.

It is submitted therefore that a proper combination of these references does not disclose the invention as now made more clear in the amended Claim 1.

The Examiner has not cited Rozanski nor Wesolowski in any

rejection of Claim 1. However for completeness we point out that:

Rozanski presents a PLL that can again be tuned and thus optimized to various conditions by storing the loop filter output in memory and under various circumstances using this stored loop filter output rather than the current loop filter output in order to improve performance. The stored output is updated from time to time to maintain a current indication of what the output should be. (see column 2) Rozanski therefore stores history based only on the output of the loop filter and not related to the internal components and storage elements making up the loop filter. History in this manner can be likened to hysteresis. However, the intent was not to store the internal register values of the loop filter and reference them to a particular one out of many input signals in a context memory as in the present invention. The present invention acts to store all necessary values making up the context of the PLL within the memory such that the PLL can be switched to service multiple different input signals simultaneously when the control logic is clocked at a high rate.

Wesolowski introduces a control function into the PLL that provides variable routing under various circumstances in order to optimize the PLL for those circumstances and to reduce transient problems upon switching between different references. For example, upon holdover numerous components making up the PLL are switched into different modes and inputs and outputs are rerouted in order to maintain the best possible frequency stability. Furthermore, the controller can control and vary the parameters of the loop filter in order to adaptively change gains etc. and thereby result in shortened phase lock

acquisition time. Those skilled in the art will be familiar with the process of adaptively switching gains and loop filter bandwidths within a PLL in order to trade off acquisition time during the transient locking phase with steady state performance. Wesolowski merely discloses that the control logic used to implement various other functions related to the invention (switching between different references and into and out of holdover mode etc) can also serve the convenient purpose of providing an implementation means for an adaptive PLL. Wesolowski does not however state or make obvious that such control logic can be utilized to simultaneously synchronize multiple input signals with a single PLL by applying a context memory to store all delay element history data for each input signal and applying a high speed clock signal to perform the functions.

Neither Rozanski nor Wesolowski thus overcome the deficiencies of the above combination of Pinto and Yamashita in respect of the present invention as now defined so that the rejection under 35 U.S.C.103 should be withdrawn.

Respectfully submitted

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April 16, 2007

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